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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,157	08/04/2003	Dirk Foerstner	10191/3299	6331
26646	7590	02/07/2007	EXAMINER	
KENYON & KENYON LLP ONE BROADWAY NEW YORK, NY 10004			LOHN, JOSHUA A	
			ART UNIT	PAPER NUMBER
			2114	
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	02/07/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/634,157	FOERSTNER ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Joshua A. Lohn	2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 22 December 2003.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-14 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-4 and 8-14 is/are rejected.  
 7) Claim(s) 5-7 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 04 August 2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |                                                                                                                                 |                                                                   |
|---------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                            | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>8/4/03</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
|                                                                                                                                 | 6) <input type="checkbox"/> Other: _____                          |

## NON-FINAL REJECTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear what is meant by the statement of "that the duration ... is less than the time interval gives a clock rate that is slightly above an upper tolerance limit." Since the first part defining the duration of the waiting loops as being less than the time interval, this portion of the claim will be examined in view of prior art for completeness. However, with regard to the portion relating to "gives a clock rate...", it is unclear how this portion relates to defining the waiting loop duration limitation or any of the claims as a whole and will not be examined with respect to prior art.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 8, 9, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Hofsäss et al., United States Patent number 5,522,040, published May 28, 1996.

As per claim 1, Hofsäss discloses a method for monitoring a microprocessor using an assigned watchdog, comprising:

causing the watchdog to monitor a reception of a reset pulse within a time interval of a predetermined duration (Hofsäss, col. 2, lines 46-52);

causing the watchdog to initiate a reset of the microprocessor if the reset pulse is not received (Hofsäss, col. 1, lines 61-62); and

executing at least one check function of the watchdog in an operating phase of the microprocessor (Hofsäss, col. 3, lines 9-33), each one of the at least one check function including a reset of the watchdog (Hofsäss, col. 3, lines 12-15, where the first pulse following the reset, like each pulse, resets the watchdog) and an execution of a sequence of waiting loops (Hofsäss, col. 3, lines 14-16, where the time count of the dead time is the sequence of waiting loops, where each clock cycle spent waiting is a waiting loop), wherein a duration of the execution of the sequence of waiting loops of at least one of the at least one check function is greater than the predetermined duration of the time interval (Hofsäss, col. 3, lines 18-22, where the dead time eventually exceeds the time interval).

As per claim 2, Hofsäss further discloses the method as recited in Claim 1, further comprising: generating an error message if the watchdog has not reset the microprocessor by an end of the sequence of waiting loops (Hofsäss, col. 4, lines 33-37).

As per claim 8, Hofsäss further discloses the method as recited in Claim 1, wherein: a number of waiting loops in the sequence of waiting loops is selected during at least one execution of the at least one check function in such a way that the duration of the execution of the sequence of waiting loops is less than the time interval (Hofsäss, col. 4, lines 51-65).

As per claim 9, Hofsäss further discloses the method as recited in Claim 1, wherein: the operating phase is at least a switching on of the microprocessor (Hofsäss, col. 3, lines 10-14).

As per claim 14, this claim is merely a computer program stored in memory for executing the methods of claim 1. Hofsäss discloses all the limitations of claim 1, as shown above. Further, Hofsäss discloses the use of a computer program to accomplish these methods (Hofsäss, col. 2, lines 41-43, where the memory storing the program is part of the microcomputer).

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofsäss in view of McCurry et al., United States patent number 5,184,025, published February 2, 1993.

As per claim 3, Hofsäss discloses the method as recited in claim 1, but fails to disclose the additional limitation relating to a counter.

McCurry discloses incrementing a counter with the execution of the at least one check function, the execution of the at least one check function being a function of a content of the counter (McCurry, col. 16, lines 45-48, where the clock acts as a counter

that is incremented with all execution, including check functions, and the check function is only executed at a predetermined clock value).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the counter of McCurry in the invention of Hofsäss.

This would have been obvious because Hofsäss discloses a desire to only test periodically as needed (Hofsäss, col. 2, line 3-9). McCurry furthers this desire by providing a method that only tests after a specific timer count of operation (McCurry, col. 16, lines 40-48.

As per claim 4, Hofsäss and McCurry further disclose the method as recited in Claim 3, further comprising: performing the at least one check function at the content of the counter (McCurry, col. 16, lines 47-48); and skipping the at least one check function at another content of the counter, the counter alternating between the content of the counter and the other content of the counter (McCurry, col. 16, lines 40-45, where all non-check times represent the other content of the counter and skip the execution of the check function).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofsäss in further view of Shonaka, United States patent number 4,809,280, published February 28, 1989.

As per claim 10, Hofsäss discloses the method as recited in claim 1, however Hofsäss fails to disclose providing multiple clock signals.

Shonaka discloses a watchdog is supplied a clock signal that differs from a clock signal of the microprocessor (Shonaka, col. 1, lines 16-18).

It would have been obvious to one of ordinary skill in the art to include the clock signals of Shonaka in the invention of Hofsäss.

This would have been obvious because Hofsäss discloses a desire to completely monitor a system (Hofsäss, col. 1, lines 30-32). Shonaka furthers this desire by providing the ability to also detect failures in the clock of the microcomputer (Shonaka, col. 1, lines 16-22).

Claims 11 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Hofsäss in view of McCurry, in further view of Shonaka.

As per claim 11, Hofsäss discloses a circuit arrangement, comprising: a microprocessor; a watchdog assigned to the microprocessor and for performing a reset of the microprocessor if a reset pulse is not received within a time interval of predetermined duration (Hofsäss, col. 1, lines 61-62, and col. 2, lines 46-52). Hofsäss further discloses a non-volatile memory to which is assigned the microprocessor, at least a test indicator is stored in the non-volatile memory (Hofsäss, col. 2, lines 3-12). Hofsäss fails to disclose a counter, whose value is the test indicator.

McCurry discloses a counter, where the value of the counter is stored to indicate test times (McCurry, col. 16, lines 45-48, where the clock acts as the counter).

It would have been obvious to one of ordinary skill in the art to include the counter of McCurry in the invention of Hofsäss.

This would have been obvious because Hofsäss discloses a desire to only test periodically as needed (Hofsäss, col. 2, line 3-9). McCurry furthers this desire by providing a method that only tests after a specific timer count of operation (McCurry, col. 16, lines 40-48).

Hofsäss and McCurry fail to disclose having different clock signals.

Shonaka discloses a watchdog is supplied a clock signal that differs from a clock signal of the microprocessor (Shonaka, col. 1, lines 16-18).

It would have been obvious to one of ordinary skill in the art to include the clock signals of Shonaka in the invention of Hofsäss and McCurry.

This would have been obvious because Hofsäss and McCurry disclose a desire to completely monitor a system (Hofsäss, col. 1, lines 30-32). Shonaka furthers this desire by providing the ability to also detect failures in the clock of the microcomputer (Shonaka, col. 1, lines 16-22).

As per claim 13, Hofsäss, McCurry and Shonaka disclose the circuit arrangement as recited in Claim 11, wherein: the non-volatile memory is a part of the microprocessor (Hofsäss, see figure 1, where the microcomputer includes memory, as is shown by block 6).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofsäss, McCurry, and Shonaka, in view of Newton's Telecom Dictionary, EEPROM definition, published February, 2002.

As per claim 12, Hofsäss, McCurry and Shonaka disclose the circuit arrangement of claim 11, however fail to explicitly disclose the use of an EEPROM.

Newton's discloses using an EEPROM (Newton's, page 258).

It would have been obvious to one of ordinary skill in the art to use the EEPROM of Newton's in the invention of Hofsäss, McCurry, and Shonaka.

This would have been obvious because Hofsäss discloses a desire for non-volatile memory without giving an explicit type to implement with (Hofsäss, col. 2, lines 10-12), and Newton's discloses that an EEPROM is common type of nonvolatile memory (Newton's, page 258).

***Allowable Subject Matter***

Claims 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is provided on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A. Lohn whose telephone number is (571) 272-3661. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAL

  
JOSHUA LOHN  
PATENT EXAMINER 2114